

15979 U.S. PRO  
09/898752  
07/03/01

826	Subclass
708	Class
ISSUE CLASSIFICATION	

516

PATENT NUMBER	
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## U.S. UTILITY Patent Application

M.S.	O.I.P.E.	PATENT DATE
SCANNED	KS2	04/01

APPLICATION NO. 09/898752	CONT/PRIOR F	CLASS 708	SUBCLASS 616	ART UNIT 2121	EXAMINER Malzahn
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APPLICANTS Sunil Talwar Dmitriy Rumyantsev	TITLE Multiplication logic circuit	PTO-2040 12/99
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## ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)		
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)	
708	626	708	210	
INTERNATIONAL CLASSIFICATION				
G 06 F 7/50				
<input type="checkbox"/> Continued on Issue Slip Inside File Jacket				

<input type="checkbox"/> TERMINAL DISCLAIMER		DRAWINGS		CLAIMS ALLOWED	
<input type="checkbox"/> The term of this patent, subsequent to _____ (date) has been disclaimed.		Sheets Drwg. 8	Figs. Drwg. 10	Print Fig. 5	Total Claims 5 /
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent No. _____		(Assistant Examiner) S. M. Malzahn		Print Claim for O.G. 1	
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.		(Primary Examiner) S. M. Malzahn DAVID H. MALZAHN PRIMARY EXAMINER (Primary Examiner) 5/22/04 (Date)		NOTICE OF ALLOWANCE MAILED 05/25/04	
				ISSUE FEE	
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## ISSUE FEE IN FILE

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